XRET5032/XRET5032C Product Brief

1. Description

The XRET5032/XRET5032C is a PCIe protocol compliant signal timer designed to ensure that the link budget meets the demanding SI requirements of expanding PCIe Gen5 channels, including PCBS, connectors and cables. By utilizing sophisticated signal conditioning methods, it compensates for channel attenuation and mitigated the effects of various jitter sources. The device features 32 Rx-Tx pairs, supports speeds of up to 32 GT/s, and provides 16-channel Retimer functionality.

2. Features

- Conform to PCIe Gen5 specifications and backward compatibility with older versions 4.0, 3.0, 2.0, 1.0.
- Compliant with the CXL standard and available in versions 1.1 and 2.0.
- Featuring channel compensation capability up to 36dB under the PCIe Gen5 standard, effectively addressing loss issues caused by PCB materials, connectors, and cables.
- Restore and conditioning , eliminate jitter form the signal.
- Adaptive equalization ability.
- Supports polarity switching, lane flipping, and AB port switching.
- Supports hot swapping.
- Support CXL sync header bypass.
- Support detect bypass mode.
- Input clock: 100MHz in standard HCSL format.
- Output clock: 100MHz standard HCSL format.
- Clock architecture：CC/SRNS/SRIS.
- Latency capability：normal mode: < 36ns，bypass mode: < 10ns.
- Supports complex bifurcation modes, including configurations such as x8 x8 and x4 x4 x4 x4, and more.
- Supports advanced data diagnostics features.
- Supports dual power planes to optimize user design: 1.8V and 0.9V.
- GUI supports temperature query, eye diagram viewing, error statistics, and more.
- Standard access interfaces: I2C, SMBus, JTAG.
- Compliant with PCIe protocol standard package.22.8mmx8.9mm, 354FCCSP, ball pitch 0.5mm.
- RoHS.

3. Applications

- Data Center
- GPU Servers
- High-Speed Interconnect

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4. Functional Diagram

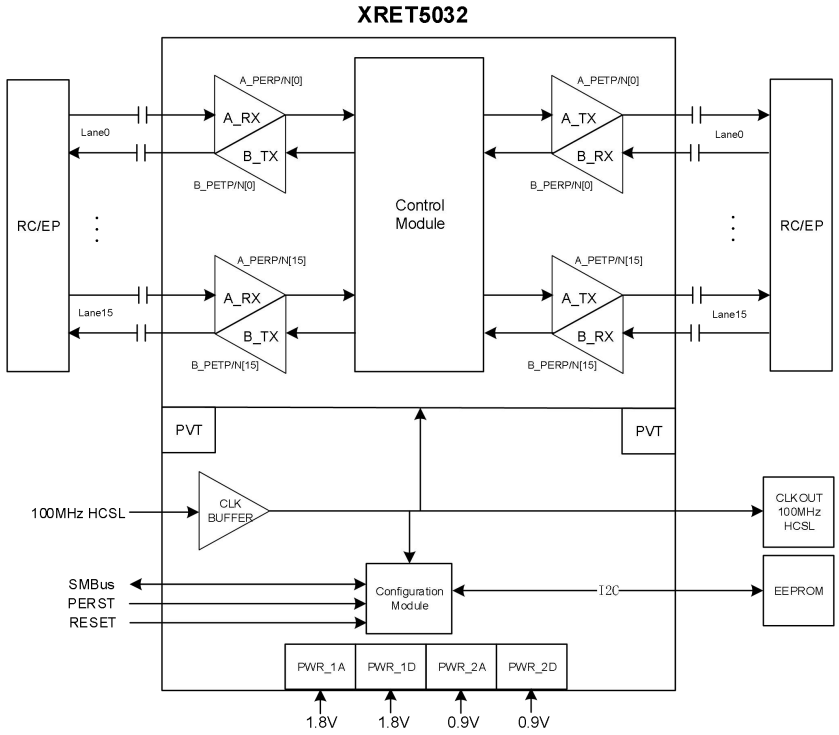

Figure 1 Functional Diagra - XRET5032

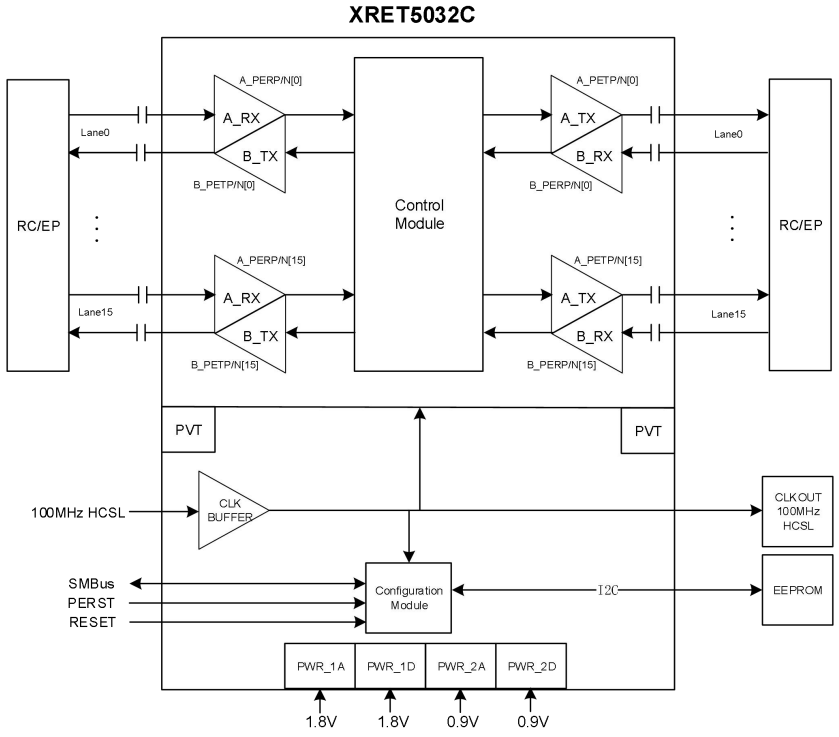

Figure 2. Functional Diagram - XRET5032C